Claim Amendments

This listing of the claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (currently amended): An integrated circuit, comprising:

a bidirectional input/output circuit; and

an input circuit for receiving a signal, said input circuit having an activation input for receiving an activation signal to activate said input circuit, in a manner dependent on the activation signal, for receiving signals, said input circuit being contained in said bidirectional input/output circuit.

Claim 2 (original): The integrated circuit according to claim 1, wherein said input circuit may be switched on or off with an aid of the activation signal.

Claims 3 (cancelled).

Claim 4 (original): The integrated circuit according to claim 1,

wherein said input circuit has a data input for a memory circuit; and

further comprising a control circuit for generating the activation signal, said control circuit generating the activation signal when data are to be written to the memory circuit through said input circuit.

Claim 5 (currently amended): ~~The integrated circuit according to claim 4, wherein~~

An integrated circuit, comprising:

an input circuit for receiving a signal, said input circuit having a data input for a memory circuit and an activation input for receiving an activation signal to activate said input circuit, in a manner dependent on the activation signal, for receiving signals; and

a control circuit for generating the activation signal, said control circuit generating the activation signal when data are to be written to the memory circuit through said input circuit;

said control circuit ~~generates~~ generating the activation signal in a manner dependent on at least one of the following signals:

a circuit select signal;

a word line activation signal;

a bit line activation signal; and

a write signal.

Claim 6 (original): The integrated circuit according to claim 1, wherein the integrated circuit is an integrated memory circuit.

Claim 7 (currently amended): A method for activating an input circuit for an integrated ~~memory~~ circuit, which comprises the step of:

providing an integrated circuit according to claim 1;

activating the input circuit if a write access has been made to the integrated ~~memory~~ circuit; and

deactivating the input circuit if the write access has not been made to the integrated ~~memory~~ circuit.